National Nuclear Security Administration
DEFENSEPROGRAMS

Computational Science Graduate Fellowship Program Review

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NNSA is a key element in the nuclear security enterprise

- Maintain a safe, secure, and reliable US nuclear stockpile
- Develop scientific understanding necessary to assess and certify weapons without underground nuclear testing
- Support a variety of threat reduction activities that rely on the capabilities and skills developed in the nuclear weapons program.

NNSA requirements are complementary to other U.S. Government needs

NNSA

- Primary focus: tightly-coupled multi-physics codes for national nuclear security decisions
- Heavily optimized code-hardware integration for efficiency
- HPC leadership ensures deterrence against adversaries

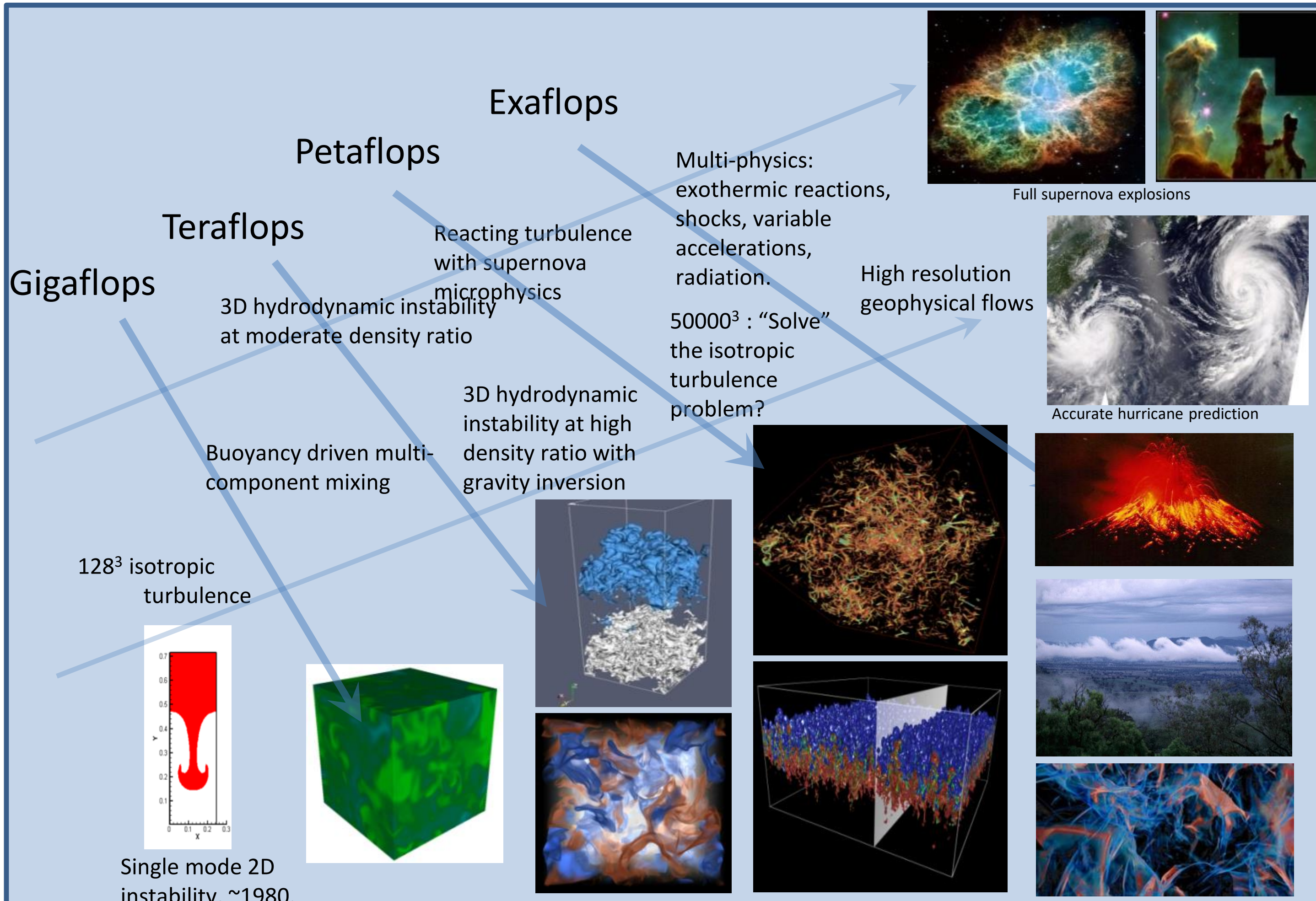
DOE/SC

- Primary focus: codes used for scientific discovery, supports broad user community
- Adapt codes to available architecture, platforms and applications developed separately
- HPC leadership leads to scientific advances on the world stage

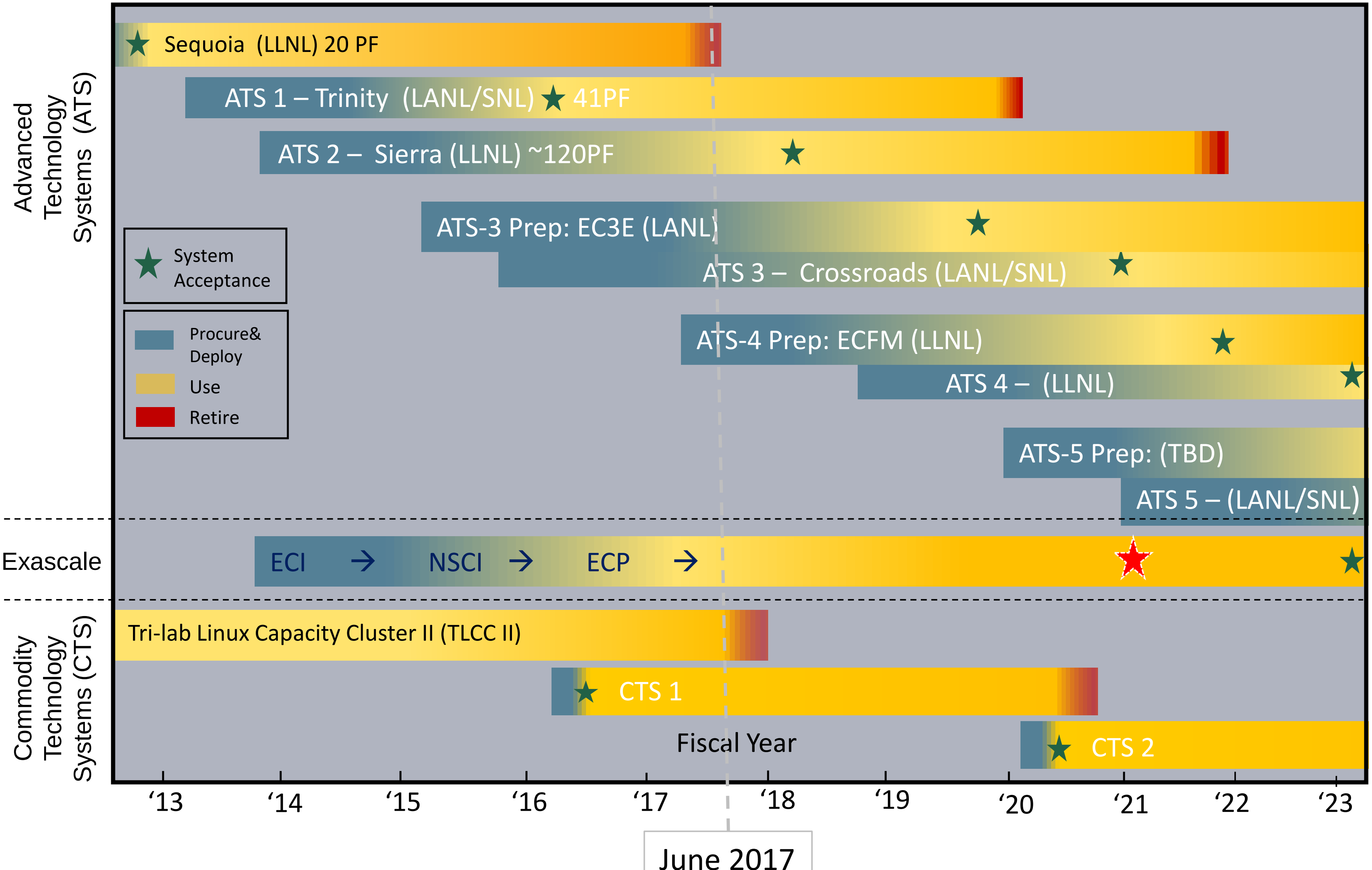
NSA

- Primary focus: data analytics and cryptography for national security
- Drives special-purpose architecture developments not necessarily efficient for NNSA and SC
- HPC leadership ensures intelligence supremacy and cyber security

Turbulence simulation is an iconic example of the need for large scale simulation

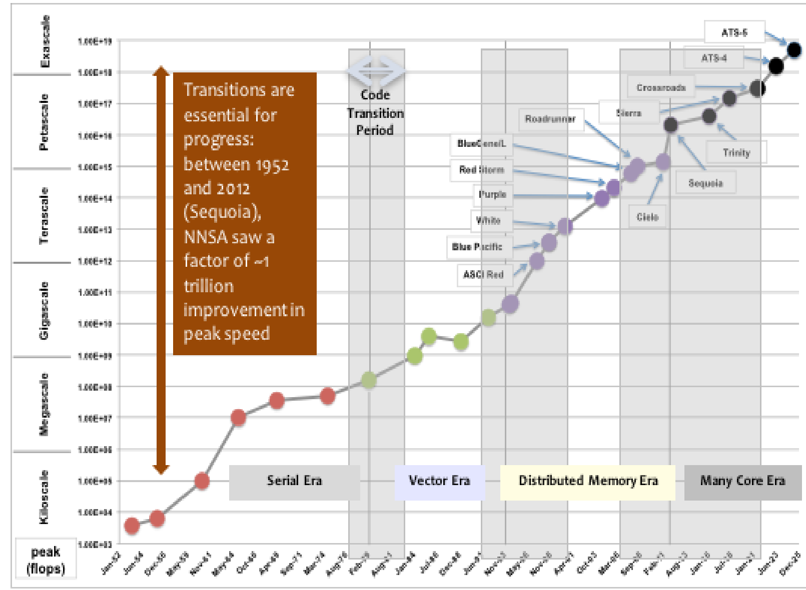


ASC Platform and Facilities Timeline



Power limitations are driving fundamental changes to architectures and programming models

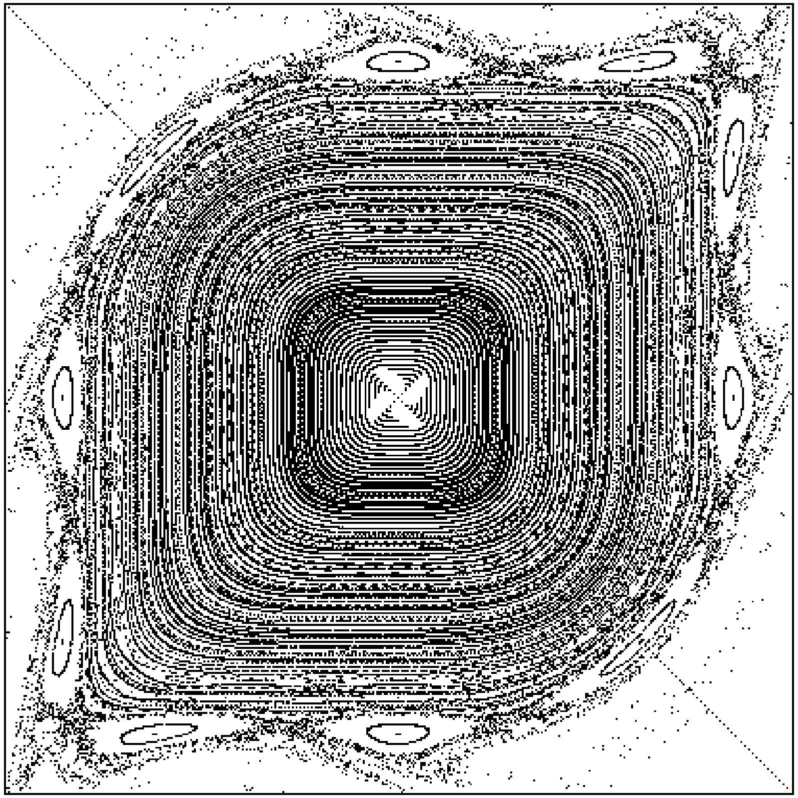
- We are entering a 4th programming model era
- Industry is migrating from FLOPS-dominated to data-movement-dominated paradigm
- Two basic system approaches:
  - Homogeneous multi-core
  - Heterogeneous (GPGPUs or ??)



Technology Challenge	Hardware Mitigation	Application Impact
Flat or decreasing processing unit (core) speeds	Dramatically increased CPU core count to track Moore's Law	First fundamental change in programming model in decades
Memory speed and capacity improvements lag far behind compute speed improvements	Multiple levels/types of memory in a CPU	Explicit management of memory placement/motion
Complex CPU designs too power-hungry to scale to exascale	Heterogeneous architectures with specialized processing units	Must coordinate both how and where specific computations are executed

The future beyond CMOS and Moore's Law holds many challenges and possibilities

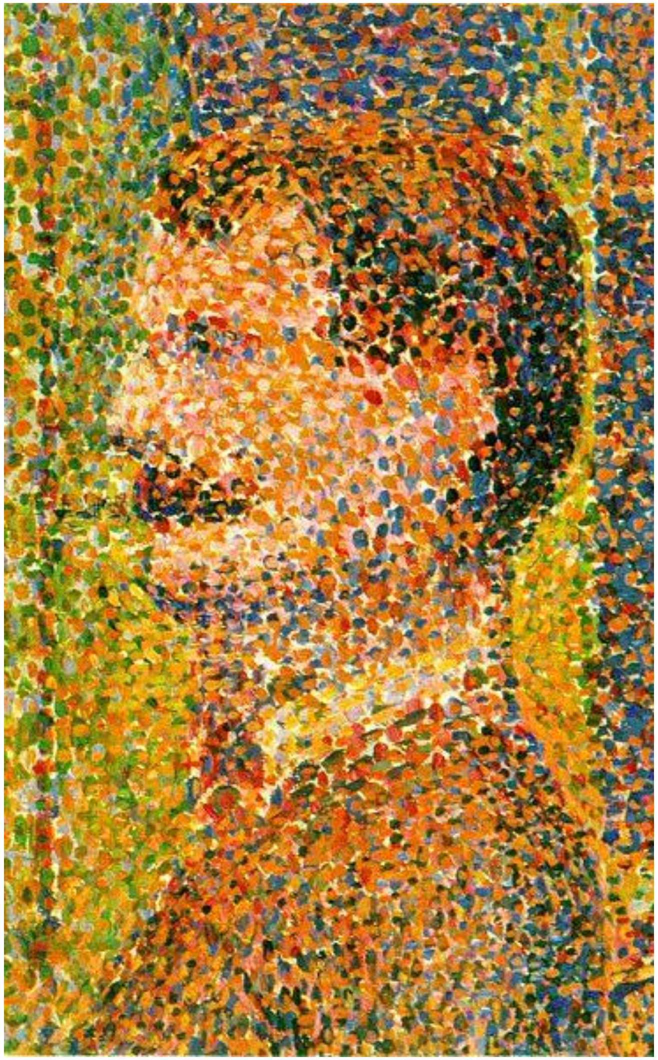
- CMOS technology is reaching some fundamental physical limits
- Alternatives to the conventional von Neumann architecture are beginning to show promise
  - Neuromorphic architectures and machine learning
  - Quantum computing



Simulations are not reality, but rather *potentially useful representations* of reality

$$\frac{BEM}{BAC} \notin \mathbb{R}$$

$$\frac{BEM}{BAC} \sim \mathbb{R}$$



Detail from *The Parade*, Georges Seurat, 1889